REMARKS

Claims 21-29 are pending in this application. Applicants respectfully request further examination and allowance of this application.

Rejections under 35 U.S.C. §103

Baliga

Claims 21-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Baliga et al. (U.S. Patent No. 4,717,679. Applicants respectfully traverse the rejection.

Claim 21 calls for a method of making a semiconductor device (e.g., 100) that includes, among other things, introducing dopants through an oxide (e.g., 103) to form a charge balancing layer (e.g., 108) within a drain of the semiconductor device and at a surface of a substrate.

The Baliga et al. reference discloses a process for fabricating an LDMOS transistor that has a p-type region 50 formed in a drain region 16, 26, 56. A metallization layer 70 electrically shorts the p-type region to the drain region. This connection scheme results in the p-type region operating as an electrode of a vertical PNP transistor that contributes substantially to the device current, as explained in column 10, lines 48-65 of the reference.

The Baliga et al. reference does not disclose introducing dopants to form a charge balancing layer within a drain of a semiconductor device. The reference is silent regarding charge balancing or forming a charge balancing

layer. P-type region 50 cannot be a charge balancing region because it is electrically shorted to drain region 16, 26, 56 by metallization layer 70. The reduction in on-resistance of the Baliga et al. device is achieved by forward biasing the junction between the p-type and drain regions to form a parallel vertical PNP transistor, not by charge balancing. As explained from page 5, line 27 to page 6, line 6 of the specification, charge balancing causes a drain voltage to induce an upward depletion into the drain from the substrate as well as a downward depletion into the drain from a charge balancing layer. This double-depletion effect allows the doping in the drain region to be increased while maintaining a high voltage breakdown, thereby reducing the on-resistance of the device. Since the Baliga et al. device has p-type region 50 and drain region 16, 26, 56 connected to each other, the potential difference between the p-type and drain regions is fixed at zero volts regardless of the drain voltage. Hence, there is no double depletion or charge balancing effect for which p-type region 50 can fairly be construed as a charge balancing layer as claimed. In effect, by preventing the double depletion effect, the Baliga et al. reference teaches away from charge balancing, forming a charge balancing layer or introducing dopants to form a charge balancing layer.

Therefore, claim 21 is believed patentable over the Baliga et al. reference. Claims 22-29 depend from an allowable base claim and therefore are allowable as well.

Accordingly, Applicant respectfully believes the rejection under 35 U.S.C. § 103 is overcome.

Conclusion

Applicants respectfully request entry of this amendment and early and favorable acceptance of this application.

Applicants have reviewed the prior art made of record and believe that such prior art does not affect the patentability of the invention.

A one month extension fee of $110.00 is believed due by filing this Amendment. However, the Commissioner is hereby authorized to charge any fees due or credit any overpayment to Deposit Account 501086.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney at the examiner's convenience.

Respectfully submitted,
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